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Quantum size impacts on the threshold voltage in nanocrystalline silicon thin film transistors

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ABSTRACT

Based on the analysis of Poisson equation, an analytical threshold voltage model including quantum size effect of nc-TFTs (nanocrystalline silicon thin film transistor) has been proposed in this paper. The results demonstrate that the proposed simplified expression of threshold voltage agree perfectly with numerical calculation. The threshold voltage in nc-TFTs strongly depends on the size of silicon grain when the size of silicon grain is less than 20 nm. Such a strong dependent relation results from the large changes in the bandgap and dielectric constant due to quantum size effects when the size of silicon grain is in the regime of nano-scale. The theoretical investigation also demonstrates that the grain boundary trap density compared to the active dopant density gives a main contribution to the threshold voltage. This implies that the grain size must be larger than 30 nm in order to avoid threshold voltage variation from different technological processes.

1. Introduction

TFTs (thin-film transistors) are used as switching elements in large-scale electronics. Polysilicon TFTs have been attracted considerable attention for large area electronics application. The evolution in materials and process fabrication technologies is rising new challenges and application areas in large-scale electronics. The nanocrystalline silicon (nc-Si) TFTs are remarkable in terms of high field effect mobility and uniformity in active matrix liquid crystal displays or active matrix organic light emitting diodes. Nc-Si TFTs have been attracted considerable attention for the active layer of the thin film transistors due to better performance and stability compared with a-Si:H TFTs [1–3]. Thus it has been proposed as promising alternatives to a-Si:H and poly-Si:H. Nc-Si TFTs are capable of both *n*- and *p*-type operation. Nc-Si has many useful advantages over a-Si:H. For example, it has increased stability due to its lower hydrogen concentration [4]. One of the most important advantages is that it can have higher mobility due to the presence of silicon crystallites [5]. Increased doping efficiency has also been demonstrated [6]. Additionally, device nonuniformity in the nc-Si:H TFTs is expected to be less significant compared to the polycrystalline silicon counterparts due to fine and uniformly-distributed silicon grains in nc-Si:H. Although the nc-Si:H TFTs currently may not attain the mobility that the polycrystalline silicon TFTs can, they are lower cost and easier to fabricate because the TFT channel layer can be deposited directly from the glow discharge of silane (SiH_4) highly diluted in hydrogen [7].

Consequently, there is a need for developing accurate model for circuit design and simulation. Therefore, it is desirable to propose a physical model. There are some semi-empirical analytical formulation of surface potential and threshold voltage for doped poly-Si TFTs have been done much [for example 8,9], whereas the study on analytical model of surface potential and threshold voltage for nc-Si TFTs is little reported. As we know, the size of nc-Si in a TFT can lead to a larger bandgap and a change in dielectric constant. In the former work [10,11], the effect of silicon grain size on the surface potential and gate leakage current of thin-film transistors has been studied. Accordingly, it is worthy to study how the size of nc-Si in a TFT under inversion bias affects on threshold voltage. In this study, firstly, a surface potential model of nc-Si TFTs including the size effects has been built to determine the electric field across the gate oxide and the surface potential in nc-Si TFTs. At last threshold voltage in nc-Si TFTs have been numerically calculated after the changes in both conduction and offset and dielectric constant due to the size effects have been considered, and an analytical model of threshold voltage for doped nc-Si TFTs is proposed.

2. Theory

In general, the 1-D Poisson equation along the *z* direction perpendicular to the substrate/gate oxide interface of TFT can be written as [12]:

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$$\frac{\partial}{\partial z}\left[\varepsilon(z)\frac{\partial \phi}{\partial z}\right] = -q\left[N_D^+(z) - N_A^-(z) + p(z) - n(z) + N_{TD}^+(z) - N_{TA}^-(z)\right] \tag{1}$$

where $\varphi(z)$ is the electrostatic potential, $\varepsilon(z)$ is spatially dependent dielectric constant, $N_D^+(z)$ and $N_A^-(z)$ are the ionized donor and acceptor concentrations, respectively, and $n(z)$ and $p(z)$ are the electron and hole densities in the nc-Si, respectively, $N_{TD}^+(z)$ is the concentration of empty (positive) grain-boundary donor traps N_{TD} at a monoenergetic level E_{TD}, $N_{TA}^-(z)$ is the concentration of occupied (negative) grain-boundary acceptor traps N_{TA} at a monoenergetic level E_{TA}; $q\varphi = E_F - E_i + q\phi_{F0}$ here, ϕ_{F0} is the Fermi potential in the film when the charge is zero [12].

$$\phi_{F0} = \frac{kT}{q}\ln\left(\frac{p_0}{n_i}\right) \tag{2}$$

where E_F is the Fermi level, and E_i is the intrinsic level (midgap). The intrinsic carrier density can be obtained as [13]

$$n_i = \frac{2(2\pi k)^{3/2}}{h^3}(m_e m_h)^{3/4} M_C^{1/2} T^{3/2}\exp\left(-\frac{E_g}{2kT}\right) \tag{3}$$

where $m_h = (m_{lh}^{3/2} + m_{hh}^{3/2})^{2/3}$, m_{lh} and m_{hh} are the light and heavy hole masses (in silicon $m_{lh} = 0.16m_0$, $m_{hh} = 0.49m_0$). In silicon $m_e = (m_l m_t^2)^{1/3}$, m_l and m_t are longitudinal and the transverse effective electron masses ($m_l = 0.98m_0$, $m_t = 0.19m_0$). Band gap E_g = 1.12 - eV. M_c is the number of equivalent minima in the conduction band (M_c = 6 for silicon). The above parameters about effective mass with the assumption that the grain size has no effect on the effective mass have been used in this paper, The trap densities N_{TA} and N_{TD} are related to the respective grain-boundary surface state (areal) density N_{ST} by $N_T = 2N_{ST}/d$, here, d is the average grain size [14]. And an active dopant concentration is defined as [8]

$$N_{Aa}^- = N_A^- - N_{TD}^+ \tag{4}$$

Using our previous method [10,11], the electric field at the interface is obtained

$$(E(\varphi_s))^2 = \frac{2q}{\varepsilon_{nc\text{-}Si}}\left(\left(N_{Aa}^- + \frac{N_{ST}}{d}\right)\varphi_s + n_0 kT\left(\exp\left(\frac{q\varphi_s}{kT}\right) - 1\right) + \frac{N_{ST}kT}{d}\ln\left(\frac{1+\exp\left(-\frac{q\varphi_s + (E_i - E_{TA} - q\phi_{F0})}{kT}\right)}{1+\exp\left(-\frac{(E_i - E_{TA} - q\phi_{F0})}{kT}\right)}\right)\right) \tag{5}$$

where $p_0 \approx N_{Aa}^-$, and $n_0 = \frac{n_i^2}{N_{Aa}^-} = \frac{1}{N_{Aa}^-}\frac{4(2\pi kT)^3(m_e m_h)^{3/2}}{h^6}\exp\left(-\frac{E_g}{kT}\right)$.

The screening dielectric constant of nc-Si can be theoretically calculated with the formula below [15]

$$\varepsilon_{nc\text{-}Si}(d) = 1 + \frac{10.4}{1 + \left(\frac{1.38}{d\times 10^9}\right)^{1.37}} \tag{6}$$

The experimental data of the bandgap of nc-Si obey with the formula below [16]

$$\Delta E_g = E_g(d) - E_g(\infty) = \frac{3.4382}{d\times 10^9} + \frac{1.1483}{\left(d\times 10^9\right)^2}\ (\text{eV}) \tag{7}$$

where $E_g(d)$ is the quantum dot bandgap as a function of radius, $E_g(\infty)$ is the bulk bandgap. In this study, Eqs. (6) and (7) have also been assumed that it can be used to describe the dielectric constant and the bandgap of poly-Si.

For the shifts of valence and conduction band-edges within the effective mass approximation can be modeled [17]

$$\frac{\Delta E_v(d)}{\Delta E_c(d)} = \frac{m_e}{m_h} \tag{8}$$

where m_h and m_e are the effective hole and electron mass, respectively. Thus

$$\Delta E_c(d) = \frac{\Delta E_g}{\left(1 + \frac{m_e}{m_h}\right)} = \frac{\frac{3.4382}{d\times 10^9} + \frac{1.1483}{(d\times 10^9)^2}}{\left(1 + \frac{m_e}{m_h}\right)}(\text{eV}) \tag{9}$$

$$\Delta E_v(d) = \frac{\Delta E_g}{\left(1 + \frac{m_h}{m_e}\right)} = \frac{\frac{3.4382}{d\times 10^9} + \frac{1.1483}{(d\times 10^9)^2}}{\left(1 + \frac{m_h}{m_e}\right)}(\text{eV}) \tag{10}$$

According to Eqs. (9) and (10), there will be a shift of valence or conduction band-edge. Thus the barrier height at the nc-Si/SiO_2 interface will decrease because it equals the barrier height at the bulk-Si/SiO_2 interface minus the shift of valence or conduction band-edge. According to the above two equations, one can clearly see the bottom of the conduction band will be affected by the size effect. Thus the barrier height will be affected.

Note the threshold voltage or turn-on voltage is defined as the voltage at which strong inversion occurs. Strong inversion begins at according to Ref. [13]

$$\varphi_s \approx 2\phi_p \approx 2\frac{kT}{q}\ln\left(\frac{N_{aa}^- + 2\frac{N_{ST}}{d}}{n_i}\right) \tag{11}$$

Thus the threshold voltage expression about can be obtained as

$$V_T = V_{FB} + 2\phi_p + \frac{\varepsilon_{nc\text{-}Si}}{\varepsilon_{ox}}t_{ox} \times\sqrt{\frac{2q}{\varepsilon_{nc\text{-}Si}}\left(\left(N_{Aa}^- + \frac{N_{ST}}{d}\right)(2\phi_p) + n_0 kT\left(\exp\left(\frac{2q\phi_p}{kT}\right) - 1\right) + \frac{N_{ST}kT}{d}\ln\left(\frac{1+\exp\left(-\frac{2q\phi_p + (E_i - E_{TA} - q\phi_{F0})}{kT}\right)}{1+\exp\left(-\frac{(E_i - E_{TA} - q\phi_{F0})}{kT}\right)}\right)\right)} \tag{12}$$

By using the strong inversion condition and the assumption that the $q\phi_s$ and $E_i - E_{TA} - q\phi_{F0}$ are much larger than of kT, the electric field from (5) is simplified to

$$\begin{aligned}(E(\varphi_s))^2 &= \frac{2q}{\varepsilon_{nc\text{-}Si}}\left(\left(N_{Aa}^- + \frac{N_{ST}}{d}\right)\phi_s + n_0 kT\exp\left(\frac{q\varphi_s}{kT}\right)\right)\\ &= \frac{2q}{\left(1 + \frac{10.4}{1+\left(\frac{1.38}{d\times 10^9}\right)^{1.37}}\right)\varepsilon_0}\\ &\quad\times\left(\left(N_{Aa}^- + \frac{N_{ST}}{d}\right)\varphi_s + \frac{4kT(2\pi kT)^3(m_e m_h)^{3/2}}{N_{Aa}^- h^6}\right.\\ &\quad\left.\exp\left(-\frac{E_g(\infty) + q\left(\frac{3.4382}{d\times 10^9} + \frac{1.1483}{(d\times 10^9)^2}\right)}{kT}\right)kT\exp\left(\frac{q\varphi_s}{kT}\right)\right)\end{aligned} \tag{13}$$

Thus the threshold voltage expression about can be obtained as

$$V_T = V_{FB} + 2\phi_p + \frac{\varepsilon_{nc\text{-}Si}}{\varepsilon_{ox}}t_{ox} \times\sqrt{\frac{2q}{\varepsilon_{nc\text{-}Si}}\left(\left(N_{Aa}^- + \frac{N_{ST}}{d}\right)(2\phi_p) + n_0 kT\exp\left(\frac{q(2\phi_p)}{kT}\right)\right)} \tag{14}$$

The precise concept of threshold voltage in undoped-body MOSFETs has been scrutinized in 2006 [18] and the parameter extraction methods have been reviewed recently [19]. It explain that threshold voltage should be understood as the crossover into the strong conduction region where the surface potential is said to be practically pinned or strong inversion begin.

3. Results and discussion

According to Ref. [8], the grain-boundary acceptor trap density, the active dopant density, and the flat band voltage have been cho-

sen as 1.0×10^{11} cm^{-2}, 1.0×10^{14} cm^{-3}, and -1.1 V, respectively. The relative dielectric constants of bulk silicon and silicon dioxide have been chosen as 11.4 and 3.9, respectively. The grain-boundary acceptor trap level energy has been chosen as $E_T - E_v = 0.15$ eV for all calculations. The gate oxide thickness of 30 nm has been used in all calculation. The bandgap of 1.12 eV for bulk silicon have been used. Using the similar method for solving Poisson equation for *n*-channel MOS structure in our previous work [20,21], numerical results on the relation between the gate voltage and surface potential can be obtained, and thus the threshold voltage can be determined according to the definition. Also note that Eq. (12) is the exact analytical solution to Poisson equation with the assumption that the hole concentration can be neglected and such an assumption is valid for the strong inversion. There is no difference between the surface potential at a given gate voltage calculated from numerical calculations and from Eq. (12). Fig. 1a demonstrates that there is no difference between both treatments. The threshold voltage or turn-on voltage is defined as the voltage at which strong inversion occurs, thus there is also no difference of threshold voltage between both treatments.

Fig. 1b gives how the size of silicon grain affects on the threshold voltage when other parameters keep constant at temperature of 300 K and 500 K. As a comparison the relation between the intrinsic carrier density and the size of silicon grain is also given in this figure. One can clearly see that the size of silicon grain will have a larger effect on the threshold voltage when the size of silicon grain is in the regime of nano-scale. With the size of silicon grain decreasing, the threshold voltage increases rapidly especially when the size of silicon grain is less than 20 nm. Such an effect results from the same trend between the intrinsic carrier density and the size of silicon grain. The results about threshold voltage obtained by both numerical solutions and a simplified analytical expression (Eq. (14)) have been plotted in Fig. 1. The results calculated from the simplified analytical expression (Eq. (14)) agree well with those from numerical solution.

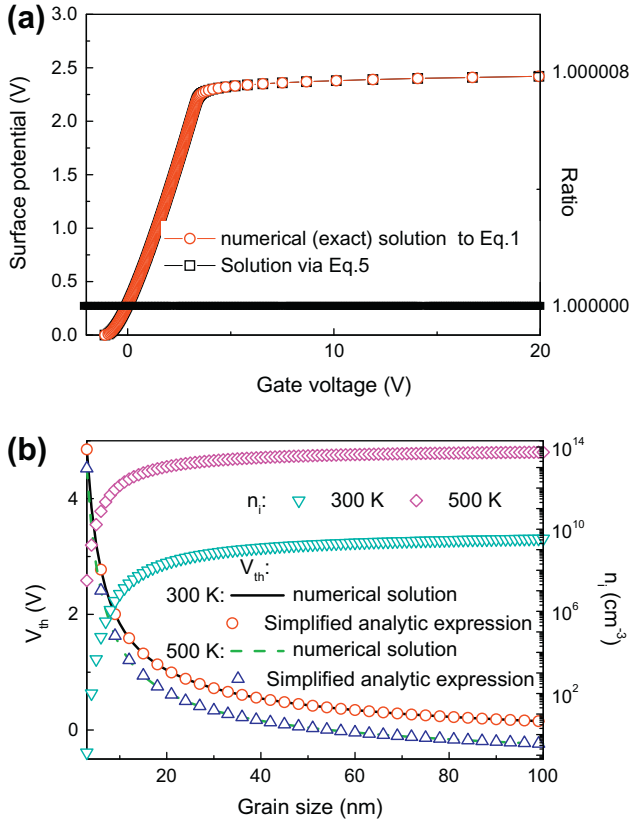

Fig. 1. (a) The comparison of surface potential between numerical (exact) solution via Eq. (1) and solution via Eq. (5) with the assumption he assumption that the hole concentration can be neglected and their ratio as a function of the gate voltage at temperature of 300 K and the grain size of 10 nm, and (b) the threshold voltage as a function of the size of silicon grain with grain-boundary acceptor trap density of 1.0×10^{11} cm^{-2}, the active dopant density of 1.0×10^{14} cm^{-3} and temperature of 300 K and 500 K. The intrinsic carrier density as a function of the size of silicon grain is also given.

Fig. 2 plots how the threshold voltage changes with temperature for different size of silicon grain. The results calculated from the analytical expression (Eq. (12)) agrees perfectly with those from numerical solution can be concluded. Fig. 2 clearly demonstrates that threshold voltage decreases with temperature increases for all sizes. This can be used to explain that the intrinsic carrier density increases with temperature increases and thus leads to a decrease in the threshold voltage.

Fig. 3 shows the effects of the silicon grain size on the threshold voltage under different active dopant density. As a comparison this figures also depicts how the bandgap changes with the size of silicon grain. One can clearly see that the active dopant density will have little effect on the threshold voltage when the size of silicon grain is few nano-meters. With the size of silicon grain increasing, the effect of the active dopant density on the threshold voltage increases. This is because the threshold voltage increases with the reciprocal of the size of silicon grain, which can be easily be seen in Eq. (14) and the effect of the active dopant density compared to that of grain boundary trap density increases. In a word, the above effects result from the change in bandgap due to the size of silicon grain. Recently experimental work [22] shows that the cross-sectional bright-field HRTEM images confirm the existence of nc-Si embedded in the a-Si host matrix grown with a RF plasma power of 20 W. The grain size distribution of nc-Si films reveals that the nc-Si grain size is ranged between 2.1 and 4.8 nm, which can be fitted by a Gaussian function with a peak at 2.7 nm and a full-width-at-half-maximum of 1.8 nm. On the other hand, the grain size distribution of nc-Si films grown with the RF plasma power of 100 W reveals that the Si-QD size distribution slightly broadens from 2.1 and 5.1 nm, which can be fitted by a Gaussian Function with a peak at 3.6 nm and a full-width-at-half-maximum of 1.5 nm. The decrement on threshold voltage of nc-Si TFTs (from 4.3 V to 2.7 V) with increasing RF plasma power (from 20 W to 100 W) has been observed. One can easily find that the average size of silicon grain grown with the RF plasma power of 20 W is smaller that of 100 W. Such experimental results agree well with the tendency of an increase in the threshold voltage with decreasing size of grain. Due to there is no relationships between the dielectric constant and the bandgap of a nc-Si grain a continuous nc-Si:H thin film, we use it is just a roughly estimation. Compare with the

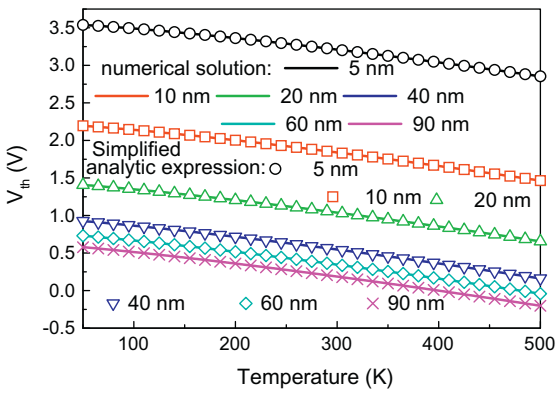

Fig. 2. The threshold voltage as a function of temperature with grain-boundary acceptor trap density of 1.0×10^{11} cm^{-2} and the active dopant density of 1.0×10^{14} cm^{-3}.

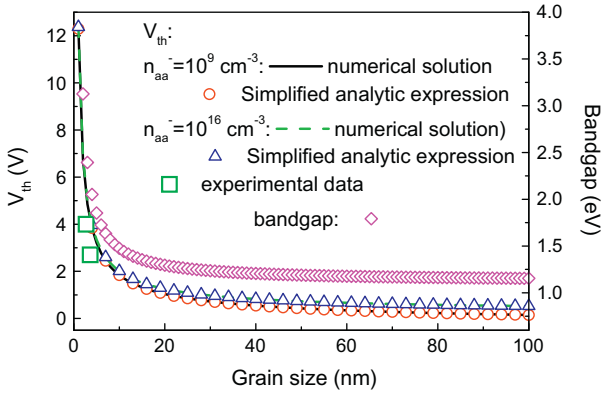

Fig. 3. The threshold voltage as a function of the size of silicon grain with grain-boundary acceptor trap density of 1.0×10^{11} cm^{-2} under temperature of 300 K for different the active dopant density. The band gap as a function of the size of silicon grain is also given.

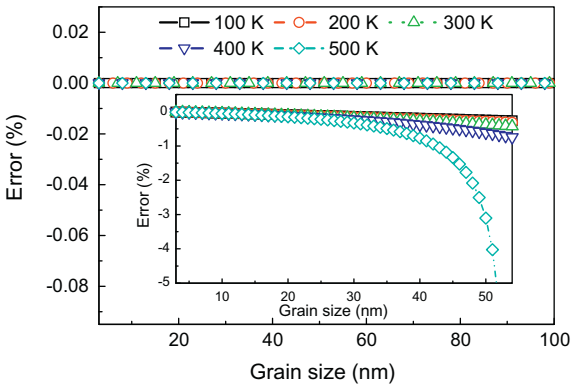

Fig. 5. The error of threshold voltage using the simplified analytical expression (Eq. (14)) as a function of the size of silicon grain with grain-boundary acceptor trap density of 1.0×10^{11} cm^{-2}, the active dopant density of 1.0×10^{14} cm^{-3} and temperature from 300 K and 500 K. The inset displays the errors of threshold voltage using the simplified analytical expression neglecting effect of the active dopant density on the threshold voltage (Eq. (15)).

experimental results in Ref. [22] via using the peak size in grain size distribution substituting the grain size, Fig. 3 shows that the experimental threshold voltage change more rapidly with the size of grain than that theoretical expectation is. Such a difference should results from the rough approximation that is using the relationship of a single nc-Si grain to substitute the relationship for the case of a continuous nc-Si:H thin film.

Fig. 4 shows how the threshold voltage changes with the active dopant density for different size of silicon grain. It can be clearly seen in this figure that the active dopant density has a very small effect on the threshold voltage in nc-Si TFTs when the active dopant density less than a special density. Such a special density increases with the size of silicon grain decreasing. For this paper, the effect of the active dopant density on the threshold voltage can be neglected when its density is less than 1.0×10^{15} cm^{-3}.

According to the above discussion, when the active dopant density can be neglected, Eq. (14) can be simplified as an equation independent of the active dopant density

$$V_T = V_{FB} + 2\phi_p + \frac{\varepsilon_{nc\text{-}Si}}{\varepsilon_{ox}} t_{ox} \times \sqrt{\frac{2q}{\varepsilon_{nc\text{-}Si}} \left(\frac{N_{ST}}{d}(2\phi_p) + n_0 kT \exp\left(\frac{q(2\phi_p)}{kT}\right)\right)} \quad (15)$$

Fig. 5 depicts how the errors of threshold voltage using Eqs. (12) and (14) changes with the size of silicon grain at different temperature. That the results calculated from the simplified analytical expression (Eq. (14)) agree perfectly with those from numerical solution for all size of silicon grain and temperature can be concluded from this figure. This figure also clearly demonstrates that the change in the threshold voltage caused by active dopant density can be neglected for nc-Si TFTs when the size of silicon grain is smaller than 50 nm. Adjusting the acceptor density in the nc-Si TFTs can control the active dopant density. This means that adjusting the acceptor density in the nc-Si TFTs will have little effects on the threshold voltage and the grain boundary trap density will give a main contribution to the threshold voltage of nc-Si TFTs.

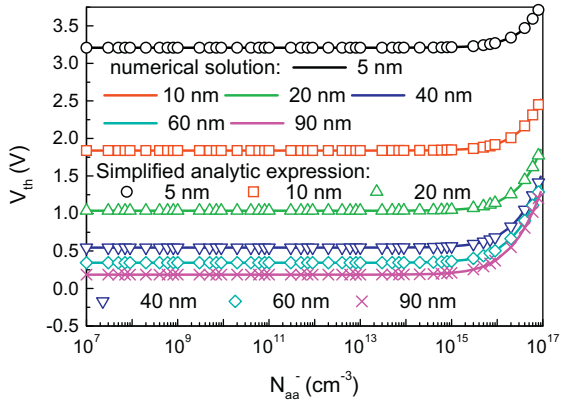

Fig. 4. The threshold voltage as a function of the active dopant density with grain-boundary acceptor trap density of 1.0×10^{11} cm^{-2} under temperature of 300 K for different values of the size of silicon grain.

4. Conclusions

Based on modeling and numerical calculation of the threshold voltage of nc-Si TFTs, the impacts of the size of silicon grain on the threshold voltage have been theoretically investigated. These results demonstrate that the proposed expression of the threshold voltage (Eq. (12)) agree perfectly with numerical calculation. The threshold voltage in nc-Si TFTs strongly depends on the size of silicon grain especially on less than 20 nm. Thus it should be given special consideration in the operation issue in TFTs and reliability issue of gate oxide when the size of silicon grain is in the regime of nano-scale. The calculations also demonstrate that the size of silicon grain impacts on the threshold voltage weakly dependently on the active dopant density. In conclusions, the main contribution to the size of silicon grain dependence of the threshold voltage in nc-Si TFTs results from the change in the bandgap and dielectric constant due to the quantum size effects.

Acknowledgments

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